47.(New) The method of claim 46, wherein forming the active circuitry includes forming a trench capacitor that extends between the second conductive material in two of the at least two second trenches.

48.(New) The method of claim 47, wherein forming the trench capacitor includes forming the trench capacitor with at least one first trench on opposite sides of the trench capacitor.

49.(New) The method of claim 44, wherein forming the communication layers in the substrate includes thinning the back side of the substrate to expose at least one of the first conductive material and the second conductive material.

REMARKS

Claims 18, 21, 24, 27, 29, 31, 33, 34, and 37-39 are amended, no claims are canceled, and claims 42-49 are added; as a result, claims 18-49 are now pending in this application.

Claim 18 is amended to remove the alphabetic characters from before the steps recited in the claims. These amendments are not made for purposes of patentablity and are not intended to alter the scope of the claim.

Claims 21, 24, 27, 29, 31, 33, 37, and 38 are amended to remove reference to alphabetic characters and refer to specific steps in parent claims. These amendments are not made for purposes of patentablity and are not intended to alter the scope of the claims.

An amendment to Fig. 1(b) is proposed to correct a reference number to correspond to the reference numbers used in the specification. Support for the proposed drawing amendment is found at specification page 5, lines 23, 24 and 36. Approval of the proposed drawing amendment is respectfully requested.

Claim Objections

Claims 27-34 were objected to for informalities. Applicant respectfully traverses these objections. The Office Action states that in claims 27, 29, 31, and 33, lines 2, 1, 2, 2, respectively, an insulative or insulating layer is used for both first and second trenches without

distinction. The appropriate use of first and second was suggested for clarity in the Office Action. Applicant believes that the claims are clear with regard to step relating the insulating layer to one of the first and second trenches. Claim 27 depends from claim 18. Claim 27 recites depositing an insulative material within each first trench over the first conductive material. Claims 29 likewise depends from claim 18. Claim 29 recites depositing an insulative material within each second trench over the second conductive material. Claim 31 likewise depends from claim 18. Claim 31 recites forming an insulating layer at the bottom of and on walls of each first trench. Claim 33 likewise depends from claim 18. Claim 33 recites forming an insulating layer at the bottom of and on walls of each second trench. Thus, claims 27, 29, 31, and 33 each depend from claim 18. Accordingly, each claim is clear as to what insulative or insulating layer is being referred to with respect to the trench in which it is formed as recited in the claims.

With respect to claim 34, applicant thanks the examiner for the suggestion that claim 34 should refer to the second trench not the first trench. Applicant so amends claim 34. This amendment is not made for purposes of patentability and is merely made to correct a minor informality in claim 34. Accordingly, claim 34 is intended to retain a full scope of equivalents.

§102 Rejection of the Claims

Claims 18, 19, 29, 31, 33, and 38-40 were rejected under 35 U.S.C. § 102(b) as being anticipated by Esquivel et al. (U.S. Patent No. 4,977,439). Applicant respectfully traverses. Claim 18 is amended to clarify the invention being claimed. Specifically, claim 18 now recites surrounding the first conductive material and the second conductive material with an insulative material to prevent short circuiting between the first conductive material and the second conductive material. Applicant can not find this feature in Esquivel et al. As all of the features of claim 18 are not found in Esquivel et al., applicant requests allowance of claim 18 and its dependent claims 19, 29, 31, 33 and 38.

With respect to claim 39, applicant respectfully traverses. Claim 39 recites surrounding the first conductive elements and the second conductive elements to prevent short circuiting. Applicant can not find these features in Esquivel et al. Accordingly, claims 39 and 40, which depends from claim 39, are believed to be allowable.

§103 Rejection of the Claims

Claims 20, 27, 28, and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Esquivel et al. Applicant respectfully traverses. The Examiner rejected claims 20, 27, 28, and 30 based only on Esquivel et al. Applicant respectfully traverses the single reference rejection under 35 U.S.C. § 103 since not all of the recited elements of the claims are found Esquivel et al. Since all the elements of the claim are not found in the reference, Applicant assumes that the Examiner is taking official notice of the missing elements. Applicant respectfully objects to the taking of official notice with a single reference obviousness rejection and, pursuant to M.P.E.P. § 2144.03, Applicant respectfully traverses the assertion of Official Notice and requests that the Examiner cite references in support of this position.

Claims 21 and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Esquivel et al. as applied to claims 18-20, 27-31, 33, and 38-40 above, in view of Liu et al. (U.S. Patent No. 6,037,257). Applicant respectfully requests withdrawal of the rejection of claims 21 and 24. Liu et al is not available as prior art against the present application. Liu et al. has a filing date of May 7, 1999. The present application is a divisional application that has an effective filing date of its parent application, Serial No. 09/069,326, of April 29, 1998. Accordingly, the present application has a filing date before the filing date of Liu et al. Withdrawal of this rejection and allowance of claims 21 and 24 are respectfully requested.

Claims 21-26 35, 36, and 41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Esquivel et al. as applied to claims 18-20, 27-31, 33, and 38-40 above, in view of Gonzales (U.S. Patent No. 5,497,017). Claims 21-26, 35, and 36 depend, at least in part, on claim 18. Applicant submits that Gonzales does not teach or suggest the features recited in claim 18 that are not found in Esquivel et al. Accordingly, applicant submits that claims 21-26, 35, and 36 are allowable with claim 18.

With respect to claim 41, applicant submits that Gonzales does not teach or suggest the features recited in claim 39 that are not found in Esquivel et al. Accordingly, applicant submits that claim 41 is allowable with claim 39.

Claims 32 and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Esquivel et al. as applied to claims 18-20, 27-31, 33, and 38-40 above, in view of Yamamoto et

al. (U.S. Patent No. 5,410,169). Applicant submits that claims 32 and 34 are allowable with their parent claim 18. Accordingly, further comment is not believed to be required.

Claim 37 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Esquivel et al. as applied to claims 18-20, 27-31, 33, and 38-40 above, in view of Gaul (U.S. Patent No. 5,646,067). Applicant submits that claim 37 is allowable with its parent claim 18. Accordingly, further comment is not believed to be required.

New claims

Claims 42-49 are added. These claims are believed to be supported by the specification. No new matter is proposed. Consideration of claims 42-49 is requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 28 May 2002 By

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 28th day of May, 2002.

Timothy Clise
Name

Signature

Docket No. 303.367US2
WD # 431504

Micron Ref. No. 97-0163.01

Clean Version of Pending Claims

BURIED CONDUCTORS
Applicant: Paul A. Farrar et al.
Serial No.: 09/930,521

Claims 18-49, as of May 28, 2002 (Date of Response to First Office Action filed).

18.(Amended) A method comprising:

forming at least one first trench within a semiconductor substrate at a first depth;

depositing a first conductive material substantially at the bottom of each first trench;

forming at least one second trench within the semiconductor substrate at a second depth shallower than the first depth;

depositing a second conductive material substantially at the bottom of each second trench; and

surrounding the first conductive material and the second conductive material with an insulative material to prevent short circuiting between the first conductive material and the second conductive material.

19. The method of claim 18, wherein the first conductive material is identical to the second conductive material.

20. The method of claim 18, wherein at least one of the first conductive material and the second conductive material comprises one of tungsten and a tungsten alloy.

21.(Amended) The method of claim 18, further comprising between forming at least one first trench and depositing a first conductive material, depositing a seed material to facilitate deposition of the first conductive material.

22. The method of claim 21, wherein the seed material comprises titanium.

23. The method of claim 21, wherein the seed material is one of an element selected from groups IVB, VB, or VIB of the periodic table.

B3

24.(Amended) The method of claim 18, further comprising between forming at least one second trench and depositing a second conductive material, depositing a seed material to facilitate deposition of the second conductive material.

25. The method of claim 24, wherein the seed material comprises titanium.

26. The method of claim 24, wherein the seed material is one of an element selected from groups IVB, VB, or VIB of the periodic table.

B4

27.(Amended) The method of claim 18, further comprising between depositing a first conductive material and forming at least one second trench, depositing an insulative material within each first trench over the first conductive material.

28. The method of claim 27, wherein the insulative material comprises silicon dioxide.

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29.(Amended) The method of claim 18, further comprising after depositing a second conductive material, depositing an insulative material within each second trench over the second conductive material.

30. The method of claim 29, wherein the insulative material comprises silicon dioxide.

31. (Amended) The method of claim 18, further comprising between forming at least one first trench and depositing a first conductive material, forming an insulating layer at the bottom of and on walls of each first trench.

32. The method of claim 31, wherein forming the insulating layer comprises oxidizing the bottom of and the walls of each first trench.

33. (Amended) The method of claim 18, further comprising between forming at least one second trench and depositing a second conductive material, forming an insulating layer at the bottom of and on walls of each second trench.

34.(Amended) The method of claim 33, wherein forming the insulating layer comprises oxidizing the bottom of and the walls of each second trench.

35. The method of claim 18, wherein at least one of the first conductive material and the second conductive material is deposited by a selective deposition process.

36. The method of claim 35, wherein the selective deposition process is selected from the group essentially consisting of chemical vapor deposition and plating.

37.(Amended) The method of claim 18, wherein the semiconductor substrate is part of a wafer having a front side and a back side, and further comprising after depositing a second conductive material, thinning the back side of the wafer to expose at least one of the first conductive material and the second conductive material.

38.(Amended) The method of claim 18, further comprising after depositing a second conductive material, connecting at least one of the first conductive material with at least one of the second conductive material.

39.(Amended) A method comprising:

burying first conductive elements within a semiconductor substrate at a first depth;

burying second conductive elements within a semiconductor substrate at a second depth less than the first depth ; and

surrounding the first conductive elements and the second conductive elements to prevent short circuiting.

40. The method of claim 39, wherein the first conductive elements and the second conductive elements each comprise a predetermined material.

41. The method of claim 39, wherein each of burying first conductive elements and burying second conductive elements comprises:

forming at least one trench within a semiconductor substrate, each trench having walls and a bottom;

forming an insulating layer at the bottom and on the walls of the trench;

depositing a seed material at the bottom of each trench;

depositing a conductive material within each trench over the seed material; and,

depositing an insulative material within each trench over the conductive material.

42 A method, comprising:

forming communication layers in a substrate;

forming an active semiconductor layer above the communication layers on the substrate; and

wherein forming the communication layers includes:

forming at least one first trench within a semiconductor substrate at a first depth;

forming an insulating layer at a bottom and sidewalls of the at least one first trench;

depositing a first seed material to facilitate deposition of a first conductive material in the at least one first trench;

depositing the first conductive material substantially at the bottom of each first trench;

forming at least one second trench within the semiconductor substrate at a second depth shallower than the first depth;

forming an insulating layer at a bottom and sidewalls of the at least one second trench;

depositing a second seed material to facilitate deposition of a second conductive material in the at least one second trench;

depositing the second conductive material substantially at the bottom of each second trench; and

forming a first insulating layer on the first conductive material to prevent short circuiting to the second conductive material.

43. The method of claim 42, wherein depositing the second conductive material includes forming a second insulating layer on the second conductive material.

44. The method of claim 43, wherein forming the active semiconductor layer includes forming the active semiconductor layer on the second insulating layer.

45. The method of claim 44, wherein forming the active semiconductor layer includes forming a P-type epitaxial layer on the second insulating layer.

46. The method of claim 45, wherein forming the active semiconductor layer includes forming an active circuitry of a semiconductor structure in the P-type epitaxial layer.

47. The method of claim 46, wherein forming the active circuitry includes forming a trench capacitor that extends between the second conductive material in two of the at least two second trenches.

48. The method of claim 47, wherein forming the trench capacitor includes forming the trench capacitor with at least one first trench on opposite sides of the trench capacitor.

49. The method of claim 44, wherein forming the communication layers in the substrate includes thinning the back side of the substrate to expose at least one of the first conductive material and the second conductive material.